Application No. 09/933,847
Amendment dated February 2, 2005
Reply to Office action of August 2, 2004
REMARKS/ARGUMENTS

On Tuesday, February 1, 2005, a change in Power of Attorney and correspondence address was filed electronically with the PTO by the Assignee of the patent application, Acorn Networks. Acorn is a company currently in bankruptcy and is represented by a Trustee, Mr. Robert O Tyler.

The Office Action of August 2, 2005 was mailed to the previous attorney at the law firm of Blakely, Sokoloff, Taylor and Zafman. The Action was unknown to the Applicant until very recently. Although the Power of Attorney change does not yet seem to be entered and does not show as recorded on PAIR, this Amendment claims its priority.

Claims 1-45 are pending in the application. None are currently allowed.

In the opinion of the inventor, the claims submitted with the original application on August 20, 2001 do not reflect the true essence or utility of the invention. Rather, they recite a specific reduction to practice and cloud the more important system context. The true essence of the invention involves the property of a microprocessor to execute an operation on arbitrary bit-fields within its operands, including the ability to generate a full set of condition codes based on this bit-field result, sufficient to enable the program to jump or branch.

The novelty of the invention is the ability of the microprocessor to effectuate the above using native instructions from its instruction set.

The utility of the invention is a significant performance speed-up in applications in which program branching depends on streaming, free-form input data such as that found in packet networks and compressed bit streams e.g. MPEG. The information in the input data stream cannot be expected to be correctly aligned when read from memory into the processor's registers.

Claims 1-28 have been re-written in light of the above. Independent claims 1 and 15 in particular has been clarified to recite the true essence of the invention.

Regarding the various prior art cited by the examiner:

In Powell et al, there is no arithmetic taking place in the ALU (or "address adder") on a bit field within an operand. There is a standard word-wise addition followed by a standard AND of the result with another register. The word size of the machine is 64 bits. Furthermore, the logical AND takes place with one operand being a special-purpose processor register, not architectural state normally under control of the programmer.

Powell and Lee et al share the common aspect of SIMD execution of "sub-operands," which is not directly related to the present invention. Configurable SIMD execution of multiple operations using the same datapath is common practice and well known to one skilled in the art. Not only addition but multiplication is possible. Both Lee's and Powell's teachings involve a reduction to practice in which a carry bit is
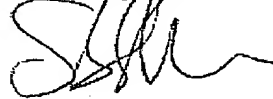
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interrupted or introduced at some point. Other techniques exist to perform SIMD arithmetic at better levels of performance, including replication of the full adder cell. One cell Ai operates as a continuation of the addition rippling through Ai-1; another cell begins a new addition at bit position i.

SIMD adders do not aim to isolate addition on a particular bit-field of interest. Rather, all bit fields are operated upon and appear in the result, whether that effect is detrimental or not. In no prior art regarding SIMD arithmetic or bit-field arithmetic, to the inventor's best knowledge, is a microprocessor able to simultaneously (e.g., at the direction of a single instruction) reconfigure its ALU to constitute an arbitrary bit-field, execute an operation on the bit field and generate the usual conditions for the field as it would a word-wise operation, and write the bit-field back to a register encapsulated by its original unmodified context bits.

Respectfully submitted,

SAM BRANDON SANDBOTE
3113 Thomas Ave #E
Dallas, TX 75204
(703) 864-8923
sandbote@sbcglobal.net